REMARKS

This Amendment seeks to place this application in condition for allowance. All of the Examiner's rejections have been addressed. Several of the pending claims have been amended. No new matter has been added.

OFFICE ACTION

In the Office Action mailed August 1, 2000, claims 151-153, 156, 159-163, 166-167, 171-172 and 174-175 were rejected as being anticipated by Japanese Laid-Open Patent Application No. 60-55459 (hereinafter "the '459 application"). The remaining claims, namely claims 154, 155, 157, 158, 164, 165, 168-170, 173, 176 and 177, were objected to as being dependent upon the rejected claims.

Rejection - 35 U.S.C. § 102:

Applicants respectfully disagree with the Examiner's position that the rejected claims are anticipated by the '459 application.[1] The Examiner stated that the '459 application discloses in figure 4, a block data transfer method and storage control method in which the number of words to be transferred is provided to memory control device

[1] The rejection here is based on prior art which similar in many respects to the prior art, namely Jackson, U.S. Patent 4,315,308, which formed the basis of the 35 U.S.C. §102 rejection made in the parent application (App. Ser. No. 09/252,997, now, U.S. Patent 6,034,918).

via bus [7](page 5, lines 11-13) and then in response to a write request (page 3, line 22), the data block is written to the destination memory area. While this may be true, memory 1 disclosed in the '459 application -- unlike the claimed invention -- is not provided nor does it receive information indicating the "number of words to transfer"[2] as required by the claims of the instant application. For example, claim 161 (as amended) recites in pertinent part:

> A method of operation in a synchronous memory device, ... the method of operation in the memory device comprises:
>
> receiving first block size information from a controller, wherein the first block size information defines a first amount of data to be input by the memory device in response to a write request

The memory in the '459 application does not receive block size information. Rather, the memory of the '459 application responds to the sequentially applied address and control signals from the memory control device 2 in order to store the appropriate number of words in memory 1.

It is the memory control device 2 of the '459 application which receives, decodes and stores the information indicating the number of words to be stored in memory 1. In this regard, the memory control device 2 stores the number of words in a counter, and, based thereon, generates and sequentially applies the appropriate address and control

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[2]For the purposes of this discussion, the phrase "number of words to transfer" may be assumed to correspond to "block size information".

signals necessary to write the words to memory 1. The information indicating the number of words to transfer is not provided to the memory (and as such, the memory does not receive such information) in the '459 application.

The '459 application

The '459 application discloses a system including memory 1, memory control device 2, cache memory 3, a main processing device 4, and an input/output processing device 5. (See Figure 2). The memory 1 is connected to memory control device 2 via memory bus 6. Memory control device 2 and input/output processing device 5 are both connected to bus 7 (See, the '459 application, page 3 lines 11-16, and Figure 2).

Communication between memory 1 and devices connected to bus 7 is executed via memory control device 2. In this regard, the '459 application states that "control of reading or writing from memory 1 is performed by memory control device 2 via memory bus 6." (page 3, line 13-14). The memory control device 2 controls memory 1 via a memory interface which includes memory address signal 242, memory data [bus] 243 and memory response signal 240. (See, the '459 application, page 6, lines 17-21). Address signal 242 and data 243 are employed to transfer address and data, respectively, between memory control device 2 and memory 1. (See, the '459 application, page 6 lines 18-21 and Figure 6).

In operation, a "number of words to transfer," together with origin and destination addresses, are provided to memory control device

2. (See, e.g., the '459 application, page 4, lines 36-39). Memory control device 2 increments or decrements source and destination address counters while maintaining a count of the number of remaining words to be transferred to memory 1. In this regard, the '459 application, on page 5, lines 21-24 states:

> The counter for the remaining number of words to transfer, which is set with number of words to transfer, is decremented each time data is transferred and stored, and when that count value reaches zero, transfer ... ends.

The memory control device 2 of the '459 application, at all times, maintains the information regarding the number of words to transfer, generates the appropriate control and address signals, and applies the control and address signals which are necessary to transfer the requested number of words to memory 1. (See, the '459 application, page 7, lines 26-39, and Figure 9). The memory control device 2 receives, decodes and stores, in a counter 203, information indicating the number of words to transfer to memory 1 and, based thereon generates address and control signals and sequentially applies those addresses and control signals in order to transfer the indicated number of words from memory 1. The memory control device 2 does <u>not</u> provide information indicating the number of words to transfer to memory 1.

Although the '459 application does not describe memory 1 in great detail,[3] memory 1 is most likely a standard off-the-shelf memory device or memory module incorporating the same, for example, memory devices like those described in the Kung et al., U.S. Pat. 4,449,207, and Voss, U.S. Pat. 4,646,270. The memory 1 described in the '459 application does not appear to input or output data synchronously with respect to a clock signal. Instead, control signals such as function signal 241 and memory response signal 240, generated by memory control device 2, are employed to signal the transfer of data between memory 1 and memory control device 2. (See, the '459 application, Figure 9, and page 7, lines 26-34). The writing of data to memory 1 from memory control device 2 is described on page 7, lines 31-34 as follows:

> ...after response 240 is acquired, if memory function signal 241 is made the write mode [ ] the contents of transfer destination address counter 203 are output as memory address signal 242, memory data 243 is transferred to and stored at the transfer destination memory area."

The '459 application Does Not Anticipate Claims 151 and 152

Claim 151 is directed to a method of controlling a memory device and requires, among other things, providing first block size information to the memory. The first block size information defines a first amount of data to be input by the memory device in response to a write request.

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[3] The '459 application suggests the use of "The latest dynamic RAMs" featuring "Nibble Mode Support" as in "*Nikkei Electronics*, April 1983." (see page 8, lines 38-39).

As mentioned above, information indicating the number of words to be transferred by the memory control device 2 is not provided to memory 1. Instead, memory control device 2 of the '459 application receives, decodes and stores that information in a counter, and, based thereon, sequentially generates the address and control signals necessary to write the words to the memory device. In this regard, the system described in the '459 application is similar to the system described in Jackson, U.S. Pat. 4,315,308. The claims of the parent (i.e., App. Ser. No. 09/252,997, now, U.S. Pat. 6,034,918) of the instant application were initially rejected as being anticipated by Jackson but ultimately found patentable over Jackson.

Importantly, memory 1 of the '459 application does not receive information indicating the number of words to be transferred. The memory 1 simply responds to the sequentially applied address and control signals provided by memory control device 2.

Thus, for at least these reasons, the '459 application does not anticipate claim 151 or the claims which depend therefrom.[4]

[4] It should be noted that claim 152 requires that the memory device input the data synchronously with respect to an external clock signal. The memory disclosed in the '459 application does not input data in this manner.

The '459 application Does Not Anticipate Claims 161 and 162

Claim 161 is directed to a method of operation in a memory device, and, like claim 151, requires that the memory device receive first block size information.

For reasons similar to those mentioned above, the memory disclosed in the '459 application does not receive the information indicating the number of words to be transferred. The memory of the '459 application simply responds to the sequentially applied address and control signals from the memory control device 2. The memory control device 2 receives, decodes and stores information that indicates the number of words to be transferred to memory 1 in a counter, and, based thereon, generates and sequentially applies the appropriate address and control signals necessary to write the appropriate number of words to memory 1. The information indicating the number of words to be transferred is not provided to memory 1.

Thus, for at least these reasons, the '459 application does not anticipate claim 161 or the claims which depend therefrom.

The '459 application Does Not Anticipate Claim 171

Claim 171 is directed to a method of operation of an integrated circuit, wherein the integrated circuit includes a memory array. Claim 171 requires, among other things, that the integrated circuit receive block size information. The memory device disclosed in the '459 application does not receive the information indicating the number of

words to transfer. Thus, for at least this reason, the '459 application does not anticipate claim 171 or its dependent claims.

CONCLUSION

Applicants request entry of the foregoing Amendment. Applicants submit that all of the claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 650-944-7772.

Respectfully submitted,

Date: October 31, 2000

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